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P Le Marrec, CA Valderrama, F Hessel, AA ... - Proceedings of the ..., 1998 - Cileseer

... The software application eliminates the **parasitic vi-**bration of the user pedal control, and the motor **behavior** vibration to have the best regulation between the pedal pres- sure and the speed of the motor. Figure 5 shows the timed co-simulation of the first example. ...

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J Mueller, R Thoma, E Demircan, C Bernicot, A ... - Solid-State Electronics, 2007 - Elsevier

... effects in the channel region were approximated with the van Dort model [8]. Consistency checks for 3D **simulation** results were available ... The following ansatz was used to model the gate voltage dependent scaling **behavior** for the different extrinsic, **parasitic** components C ...

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[berkeley.edu](#) [PS]

EWY Liu - 1993 - embedded.eecs.berkeley.edu

... The first phase in this step is component extraction where a schematic with **parasitic** resistances and capacitances is produced from layout. ... determined using SPICE **simulation**. ... of data analysis to fit parameters for **behavioral** models of the components. This identi- ...

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Patch leaving decision rules and the Marginal Value Theorem: an experimental analysis and a simulation model

[oxfordjournals.o](#)

E Wajnberg, X Fauvergue, O Pons - Behavioral Ecology, 2005 - ISBE

... a basis for building a **simulation** model of patch exploitation in **parasitic** wasps has ... **simulation**, and from the moment the female entered the patch, the **behavioral** sequence was ... The **simulation** model was first used with the regression parameters estimated from the experimental ...

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... Through the use of the code, additional insights into the plasma **behavior** are obtained and ... multiple section circuit is displayed in Figure 4, (For simplicity, the **parasitic** inductances and ... D. **Simulation Validation** Thruster modeling addressed operation at 12.8g/s varying the power ...

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K Shastri, S Pashak, P Goelsoekar, P ... - US Patent App. 11/ ..., 2006 - Google Patents

... The annotated results (complete with definitions of **parasitic** capacitances and resistances, for
example) is then re-simulated and compared with the prior **simulation**, with alterations made
 in the logic design and ... [0029] Once the **co-verification** and **co-simulation** pro-cesses ...
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A Ghotranji, F Javaheri, S Safari, Z Navabi - nad.ut.ac.ir

... **Co-Verification**: Many formal verification tools can process HDL assertions. ... Changes in parameters
 of PSO algorithm can have a **parasitic** impact on the results or the ... **Simulation** times were
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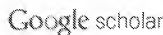
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MS McCorquodale, FH Gebara, KL Kraver, ... - Proceedings of the ..., 2003 - portal.acm.org
 ... fast as it was described by behavioral HDL, not a complete device-level netlist. ... Similarly, parasitic extraction and backannota-tion afforded an iterative process in completing the mechanical ... closure was reached in each domain, a second cross-domain simulation was executed ...

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M Etharion, J Willemsen, W Wilkening, N Ou, S ... - Microelectronics ..., 2007 - Elsevier
 ... The simulation results achieved with the original netlist without parasitic elements and applying standard device models agreed only partly with the failure modes observed from functional measurements. Some clear disagreements were observable. ...

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N Meneses, C Kashyap, C Amin - Proceedings of the 45th annual ..., 2008 - portal.acm.org
 ... Since macromodels provide us the ability to model large extracted cell netlists with only a few nonlinear current sources and capacitors, we observe significant speed-ups when using ... The larger the library cell, the more the number of parasitic elements in the extracted netlist. ...

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R Zhan, H Xie, H Feng, A Wang - Proceedings of the 2005 Asia and ..., 2005 - portal.acm.org
 ... In this paper, we present a new ESD CAD tool, entitled ESDZapper, to find the critical discharging path under ESD stress, hence, perform full-chip ESD zapping test in simulation. ... Netlist with all intentional & parasitic ESD devices ESDCat ...

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[Transistor-level timing and simulator and power analyzer](#)

X Huang, WH Zheng - US Patent 6,563,008, 1998 - Google Patents
 ... 3, 1998 Sheet 9 of 19 START J y-270 SET nCOUNT= .272 OBTAIN n FROM NETLIST BASED ON nCOUNT 274 276 CALL ... Switch-level timing simulation, represented by such pro- 35 grams as MOTIS and RSIM, serves a critical role in the simulation and verification of logic ...

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C Retyea - Communication Systems: Design, 2003 - eetindia.co.in

... To address this problem, hierarchy in the post- parasitic netlists needs to be preserved as much ... design environment, such as selecting an individual net and viewing the associated parasitic capacitance and ... Since only the block's parasitics are added to the netlist, the result is a ...

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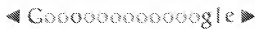
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... for holding rules that determine parasitic resis- effective when it is desired to carry out the simulation at high tances and parasitic capacitances occurring among the ele- speed without

giving great importance to the precision of the 35 merits, **net list**-forming means ...

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 ... From a comparison of the pulses in cases (i) and (iii), we see that self inductance causes the pulse to have a steep initial slope. ... **Simulation results** are shown in Fig. ... Thus, the magnitude of crosstalk slowdown may increase when parasitic inductances are considered. ...
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 ... The model is run by assuming that the population **parasite** distribution is initially at equilibrium. ... are sufficiently close to the actual benefits to warrant using the model to **compare** the potential ... The **simulation** shows a decrease in the intensity of infection over the 20 years of ...
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 ... The influence of stray inductance is shown on Fig. 12, where comparison of **results of simulation** with and without Saber® macro component generated in InCa is presented. On the other side **parasitic** capacitances of copper track can be removed. ...
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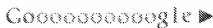
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
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